FEATURES:

- **Monolithic Flash + SRAM ComboMemory**
  - SST31LF041/041A: 512K x8 Flash + 128K x8 SRAM
  - SST31LF043/043A: 512K x8 Flash + 32K x8 SRAM

- **Single 3.0-3.6V Read and Write Operations**

- **Concurrent Operation**
  - Read from or write to SRAM while Erase/Program Flash

- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention

- **Low Power Consumption:**
  - Active Current: 10 mA (typical) for Flash and 20 mA (typical) for SRAM Read
  - Standby Current: 10 µA (typical)

- **Flash Sector-Erase Capability**
  - Uniform 4 KByte sectors

- **Latched Address and Data for Flash**

- **Fast Read Access Times:**
  - SST31LF041/043: Flash: 70 ns
  - SST31LF041A/043A: Flash: 300 ns

- **Flash Fast Erase and Byte-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Bank-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14 µs (typical)
  - Bank Rewrite Time: 8 seconds (typical)

- **Flash Automatic Erase and Program Timing**
  - Internal VPP Generation

- **Flash End-of-Write Detection**
  - Toggle Bit
  - Data# Polling

- **CMOS I/O Compatibility**

- **JEDEC Standard Command Set**

- **Packages Available**
  - 32-lead TSOP (8 x 14 mm) SST31LF041A/043A
  - 40-lead TSOP (10 x 14 mm) SST31LF041/043

PRODUCT DESCRIPTION

The SST31LF041/041A/043/043A devices are a 512K x8 CMOS flash memory bank combined with a 128K x8 or 32K x8 CMOS SRAM memory bank manufactured with SST's proprietary, high performance SuperFlash technology. The SST31LF041/041A/043/043A devices write (SRAM or flash) with a 3.0-3.6V power supply. The monolithic SST31LF041/041A/043/043A devices conform to Software Data Protect (SDP) commands for x8 EEPROMs.

Featuring high performance Byte-Program, the flash memory provides a maximum Byte-Program time of 20 µsec. The entire flash memory bank can be erased and programmed byte-by-byte in typically 8 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent flash write, the SST31LF041/041A/043/043A devices have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST31LF041/041A/043/043A devices are offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST31LF041/041A/043/043A operate as two independent memory banks with respective bank enable signals. The SRAM and Flash memory banks are superimposed in the same memory address space. Both memory banks share common address lines, data lines, WE# and OE#. The memory bank selection is done by memory bank enable signals. The SRAM bank enable signal, BES# selects the SRAM bank and the flash memory bank enable signal, BEF# selects the flash memory bank. The WE# signal has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The SDP command sequence protects the data stored in the flash memory bank from accidental alteration.

The SST31LF041/041A/043/043A provide the added functionality of being able to simultaneously read from or write to the SRAM bank while erasing or programming in the flash memory bank. The SRAM memory bank can be read or written while the flash memory bank performs Sector-Erase, Bank-Erase, or Byte-Program concurrently. All flash memory Erase and Program operations will automatically latch the input address and data signals and complete the operation in background without further input stimulus requirement. Once the internally controlled Erase or Program cycle in the flash bank has commenced, the SRAM bank can be accessed for Read or Write.

The SST31LF041/041A/043/043A devices are suited for applications that use both nonvolatile flash memory and volatile SRAM memory to store code or data. For all system applications, the SST31LF041/041A/043/043A...
devices significantly improve performance and reliability, while lowering power consumption, when compared with multiple chip solutions. The SST31LF041/041A/043/043A inherently use less energy during Erase and Program than alternative flash technologies. When programming a flash device, the total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter Erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The monolithic ComboMemory eliminates redundant functions when using two separate memories of similar architecture; therefore, reducing the total power consumption.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

The SST31LF041/041A/043/043A devices also improve flexibility by using a single package and a common set of signals to perform functions previously requiring two separate devices. To meet high density, surface mount requirements, the SST31LF041/043 device is offered in 40-lead TSOP package and the SST31LF041A/043A device is offered in 32-lead TSOP package. See Figures 1 and 2 for the pinouts.

**Device Operation**

The ComboMemory uses BES# and BEF# to control operation of either the SRAM or the flash memory bank. Bus contention is eliminated as the monolithic device will not recognize both bank enables as being simultaneously active. If both bank enables are asserted (i.e., BEF# and BES# are both low), the BEF# will dominate while the BES# is ignored and the appropriate operation will be executed in the flash memory bank. SST does not recommend that both bank enables be simultaneously asserted. All other address, data, and control lines are shared which minimizes power consumption and area. The device goes into standby when both bank enables are raised to V_HIC. See Table 3 for SRAM operation mode selection.

**SRAM Operation**

With BES# low and BEF# high, the SST31LF041/041A operate as a 128K x 8 CMOS SRAM and the SST31LF043/043A operate as 32K x 8 CMOS SRAM, with fully static operation requiring no external clocks or timing strobes. The SRAM is mapped into the first 128 KByte address space of the device for 041/041A or 32 KByte for 043/043A. Read and Write cycle times are equal.

**SRAM Read**

The SRAM Read operation of the SST31LF041/041A/043/043A are controlled by OE# and BES#, both have to be low with WE# high, for the system to obtain data from the outputs. BES# is used for SRAM bank selection. When BES# and BEF# are high, both memory banks are deselected. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. See Figure 3 for the Read cycle timing diagram.

**SRAM Write**

The SRAM Write operation of the SST31LF041/041A/043/043A is controlled by WE# and BES#; both have to be low for the system to write to the SRAM. BES# is used for SRAM bank selection. During the Byte-Write operation, the addresses and data are referenced to the rising edge of either BES# or WE#, whichever occurs first. The Write time is measured from the last falling edge to the first rising edge of BES# and WE#. OE# can be V_IL or V_IH, but no other value, for SRAM Write operations. See Figure 4 for the SRAM Write cycle timing diagram.

**Flash Operation**

With BEF# active, the SST31LF041/041A/043/043A operate as a 512K x 8 flash memory. The flash memory bank is read using the common address lines, data lines, WE# and OE#. Erase and Program operations are initiated with the JEDEC standard SDP command sequences. Address and data are latched during the SDP commands and internally timed Erase and Program operations. See Table 3 for flash operation mode selection.

**Flash Read**

The Read operation of the SST31LF041/041A/043/043A devices are controlled by BEF# and OE#; both have to be low, with WE# high, for the system to obtain data from the outputs. BEF# is used for flash memory bank selection. When BEF# and BES# are high, both banks are deselected and only standby power is consumed. OE# is the
output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. See Figure 5 for the Read cycle timing diagram.

**Flash Erase/Program Operation**

SDP commands are used to initiate the flash memory bank Program and Erase operations of the SST31LF041/041A/043/043A. SDP commands are loaded to the flash memory bank using standard microprocessor write sequences. A command is loaded by asserting WE# low while keeping BEF# low and OE# high. The address is latched on the falling edge of WE# or BEF#, whichever occurs last. The data is latched on the rising edge of WE# or BEF#, whichever occurs first.

**Flash Byte-Program Operation**

The flash memory bank of the SST31LF041/041A/043/043A devices are programmed on a byte-by-byte basis. Before the Program operations, the memory must be erased first. The Program operation consists of three steps. The first step is the three-byte-load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 µs. See Figures 6 and 7 for WE# and BEF# controlled Program operation timing diagrams and Figure 17 for flowcharts. During the Program operation, the only valid Flash Read operations are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any SDP commands loaded during the internal Program operation will be ignored.

**Flash Sector-Erase Operation**

The Sector-Erase operation allows the system to erase the flash memory bank on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KBytes. The Sector-Erase operation is initiated by executing a six-byte-command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The address lines A18-A12 will be used to determine the sector address. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 10 for timing waveforms. Any SDP commands loaded during the Sector-Erase operation will be ignored.

**Flash Bank-Erase Operation**

The SST31LF041/041A/043/043A flash memory bank provides a Bank-Erase operation, which allows the user to erase the entire flash memory bank array to the “1s” state. This is useful when the entire bank must be quickly erased. The Bank-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Bank-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or BEF# pulse, whichever occurs first. During the internal Erase operation, the only valid Flash Read operations are Toggle Bit and Data# Polling. See Table 4 for the command sequence, Figure 11 for timing diagram, and Figure 20 for the flowchart. Any SDP commands loaded during the Bank-Erase operation will be ignored.

**Flash Write Operation Status Detection**

The SST31LF041/041A/043/043A flash memory bank provides two software means to detect the completion of a flash memory bank Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit Read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ7 or DQ6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

**Flash Data# Polling (DQ7)**

When the SST31LF041/041A/043/043A flash memory bank is in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. The flash memory bank is then ready for the next operation. During internal Erase operation, any attempt to read DQ7 will produce a ‘0’. Once the internal Erase operation is completed, DQ7 will produce a ‘1’. The Data# Polling is valid after the rising edge of the fourth WE#
(or BEF#) pulse for Program operation. For Sector or Bank-Erase, the Data# Polling is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 8 for Data# Polling timing diagram and Figure 18 for a flowchart.

Flash Toggle Bit (DQ₆)
During the internal Program or Erase operation, any consecutive attempts to read DQ₆ will produce alternating 0s and 1s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The flash memory bank is then ready for the next operation. The Toggle Bit is valid after the rising edge of the fourth WE# (or BE#) pulse for Program operation. For Sector or Bank-Erase, the Toggle Bit is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 9 for Toggle Bit timing diagram and Figure 18 for a flowchart.

Flash Memory Data Protection
The SST31LF041/041A/043/043A flash memory bank provides both hardware and software features to protect non-volatile data from inadvertent writes.

Flash Hardware Data Protection
Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

VDD Power Up/Down Detection: The Write operation is inhibited when VDD is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Flash Write operation. This prevents inadvertent writes during power-up or power-down.

Flash Software Data Protection (SDP)
The SST31LF041/041A/043/043A provide the JEDEC approved Software Data Protection scheme for all flash memory bank data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence. The SST31LF041/041A/043/043A devices are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid SDP commands will abort the device to the Read mode, within TRC.

Concurrent Read and Write Operations
The SST31LF041/041A/043/043A provide the unique benefit of being able to read from or write to SRAM, while simultaneously erasing or programming the Flash. The device will ignore all SDP commands when an Erase or Program operation is in progress. This allows data alteration code to be executed from SRAM, while altering the data in Flash. The following table lists all valid states. SST does not recommend that both bank enables, BEF# and BES#, be simultaneously asserted.

Concurrent Read/Write State Table

<table>
<thead>
<tr>
<th>Flash</th>
<th>SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program/Erase</td>
<td>Read</td>
</tr>
<tr>
<td>Program/Erase</td>
<td>Write</td>
</tr>
</tbody>
</table>

Note that Product Identification commands use SDP; therefore, these commands will also be ignored while an Erase or Program operation is in progress.

Product Identification
The product identification mode identifies the devices as either SST31LF041/043 or SST31LF041A/043A and the manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware device ID Read operation is typically used by a programmer to identify the correct algorithm for the SST31LF041/041A/043/043A flash memory banks. Users may wish to use the software product identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation. Figure 12 for the software ID entry and read timing diagram and Figure 19 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

<table>
<thead>
<tr>
<th>Manufacturer's ID</th>
<th>Address</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device ID</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SST31LF041</td>
<td>0001H</td>
<td>17H</td>
</tr>
<tr>
<td>SST31LF041A</td>
<td>0001H</td>
<td>16H</td>
</tr>
<tr>
<td>SST31LF043</td>
<td>0001H</td>
<td>65H</td>
</tr>
<tr>
<td>SST31LF043A</td>
<td>0001H</td>
<td>66H</td>
</tr>
</tbody>
</table>

Product Identification Mode Exit/Reset
In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Exit ID command sequence,
which returns the device to the Read operation. Please note that the software-reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 13 for timing waveform and Figure 19 for a flowchart.

**Design Considerations**

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between VDD and VSS, e.g., less than 1 cm away from the VDD pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from VDD to VSS should be placed within 1 cm of the VDD pin.

**FIGURE 1: PIN ASSIGNMENTS FOR 40-LEAD TSOP (10MM X 14MM) - SSTLF041/043**

**FUNCTIONAL BLOCK DIAGRAM**

```
    Address Buffers          SRAM
     |                        |
BES#                          |
|                           |
BEF#                          |
|                          |
O E#                          |
|                          |
WE#                          |
|                          |
Address Buffers & Latches     SuperFlash Memory
    |                        |
AMS - A0         |
```

AMS = Most Significant Address

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### FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD TSOP (8MM X 14MM) - SSTLF041A/043A

### TABLE 2: PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin Name</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>A&lt;sub&gt;MS&lt;/sub&gt;-A&lt;sub&gt;0&lt;/sub&gt;</td>
<td>Address Inputs</td>
<td>To provide memory addresses. A&lt;sub&gt;18&lt;/sub&gt;-A&lt;sub&gt;0&lt;/sub&gt; to provide flash address A&lt;sub&gt;16&lt;/sub&gt;-A&lt;sub&gt;0&lt;/sub&gt; to provide SRAM addresses for SST32LF041/041A A&lt;sub&gt;14&lt;/sub&gt;-A&lt;sub&gt;0&lt;/sub&gt; to provide SRAM addresses for SST31LF043/043A During flash Sector-Erase, A&lt;sub&gt;18&lt;/sub&gt;-A&lt;sub&gt;12&lt;/sub&gt; address lines will select the sector.</td>
</tr>
<tr>
<td>DQ&lt;sub&gt;7&lt;/sub&gt;-DQ&lt;sub&gt;0&lt;/sub&gt;</td>
<td>Data Input/output</td>
<td>To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when OE# or BES# and BEF# are high.</td>
</tr>
<tr>
<td>BES#</td>
<td>SRAM Memory Bank Enable</td>
<td>To activate the SRAM memory bank when BES# is low. Note: For SST31LF041A/043A, BES# and OE# share pin 32.</td>
</tr>
<tr>
<td>BEF#</td>
<td>Flash Memory Bank Enable</td>
<td>To activate the Flash memory bank when BEF# is low.</td>
</tr>
<tr>
<td>OE#</td>
<td>Output Enable</td>
<td>To gate the data output buffers. Note: For SST31LF041A/043A, BES# and OE# share pin 32.</td>
</tr>
<tr>
<td>WE#</td>
<td>Write Enable</td>
<td>To control the Write operations.</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Power Supply</td>
<td>3.0-3.6V Power Supply</td>
</tr>
<tr>
<td>V&lt;sub&gt;SS&lt;/sub&gt;</td>
<td>Ground</td>
<td></td>
</tr>
</tbody>
</table>

1. A<sub>MS</sub> = Most significant address
TABLE 3: OPERATION MODES SELECTION

<table>
<thead>
<tr>
<th>Mode</th>
<th>BES#¹</th>
<th>BEF#¹</th>
<th>OE#</th>
<th>WE#</th>
<th>A₉</th>
<th>DQ</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash</td>
<td>X²</td>
<td>VᵢL</td>
<td>VᵢL</td>
<td>VᵢH</td>
<td>AᵢN</td>
<td>D_OUT</td>
<td>AᵢN</td>
</tr>
<tr>
<td>Read</td>
<td></td>
<td></td>
<td>VᵢL</td>
<td>VᵢH</td>
<td>AᵢN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Program</td>
<td></td>
<td></td>
<td>VᵢL</td>
<td>VᵢH</td>
<td>AᵢN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Erase</td>
<td></td>
<td></td>
<td>VᵢL</td>
<td>VᵢH</td>
<td>AᵢN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRAM</td>
<td>VᵢL</td>
<td>VᵢH</td>
<td>VᵢL</td>
<td>VᵢH</td>
<td>AᵢN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Write</td>
<td>VᵢL</td>
<td>VᵢH</td>
<td>X</td>
<td>VᵢL</td>
<td>AᵢN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standby</td>
<td>VᵢHC</td>
<td>VᵢHC</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>High Z</td>
<td>X</td>
</tr>
<tr>
<td>Flash Write Inhibit</td>
<td>X</td>
<td>X</td>
<td>VᵢL</td>
<td>X</td>
<td>X</td>
<td>High Z/D_OUT</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
<td>VᵢH</td>
<td>X</td>
<td>X</td>
<td>High Z/D_OUT</td>
<td>X</td>
</tr>
<tr>
<td>Product Identification</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hardware Mode</td>
<td>X</td>
<td>VᵢL</td>
<td>VᵢL</td>
<td>VᵢH</td>
<td>VᵢH</td>
<td></td>
<td>Manufacturer's ID (BFH)</td>
</tr>
<tr>
<td>Software Mode</td>
<td>X</td>
<td>VᵢL</td>
<td>VᵢL</td>
<td>VᵢH</td>
<td>AᵢN</td>
<td></td>
<td>Device ID²,ID Code</td>
</tr>
</tbody>
</table>

1. BES# and BEF# cannot be asserted simultaneously. For SST31LF041A/043A BES# and OE# share pin 32.
2. X can be VᵢL or VᵢH, but no other value.
3. Device ID 17H for SST31LF041, 16H for SST31LF041A, 65H for SST31LF043 and 66H for SST31LF043A.

TABLE 4: SOFTWARE COMMAND SEQUENCE

<table>
<thead>
<tr>
<th>Command Sequence</th>
<th>1st Bus Write Cycle</th>
<th>2nd Bus Write Cycle</th>
<th>3rd Bus Write Cycle</th>
<th>4th Bus Write Cycle</th>
<th>5th Bus Write Cycle</th>
<th>6th Bus Write Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Addr¹</td>
<td>Data</td>
<td>Addr¹</td>
<td>Data</td>
<td>Addr¹</td>
<td>Data</td>
</tr>
<tr>
<td>Byte-Program</td>
<td>5555H</td>
<td>AAH</td>
<td>2AAAH</td>
<td>55H</td>
<td>5555H</td>
<td>A0H</td>
</tr>
<tr>
<td>Sector-Erase</td>
<td>5555H</td>
<td>AAH</td>
<td>2AAAH</td>
<td>55H</td>
<td>5555H</td>
<td>80H</td>
</tr>
<tr>
<td>Bank-Erase</td>
<td>5555H</td>
<td>AAH</td>
<td>2AAAH</td>
<td>55H</td>
<td>5555H</td>
<td>80H</td>
</tr>
<tr>
<td>Software ID Entry²,⁵</td>
<td>5555H</td>
<td>AAH</td>
<td>2AAAH</td>
<td>55H</td>
<td>5555H</td>
<td>90H</td>
</tr>
<tr>
<td>Software ID Exit</td>
<td>5555H</td>
<td>AAH</td>
<td>2AAAH</td>
<td>55H</td>
<td>5555H</td>
<td>F0H</td>
</tr>
</tbody>
</table>

1. Address format A₁₄-A₀ (Hex). Address A₁₅-A₁₈ can be VᵢL or VᵢH, but no other value, for the Command sequence.
2. BA = Program Byte address
3. SAₓ for Sector-Erase; uses A₁₈-A₁₂ address lines
4. The device does not remain in Software Product ID Mode if powered down.
5. With A₁₈-A₁ =0; SST Manufacturer's ID= BFH, is read with A₀ = 0,
   SST31LF041 Device ID = 17H, is read with A₀ = 1,
   SST31LF041A Device ID = 16H, is read with A₀ = 1
   SST31LF043 Device ID = 65H, is read with A₀ = 1
   SST31LF043A Device ID = 66H, is read with A₀ = 1
**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature ................................................................. -20°C to +85°C
Storage Temperature ................................................................. -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ................................ -0.5V to VDD+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ............. -1.0V to VDD+1.0V
Voltage on A9 Pin to Ground Potential ...................................... -0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C) ......................... 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) .................... 240°C
Output Short Circuit Current1 ..................................................... 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

**OPERATING RANGE**

<table>
<thead>
<tr>
<th>Range</th>
<th>Ambient Temp</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>3.0-3.6V</td>
</tr>
<tr>
<td>Extended</td>
<td>-20°C to +85°C</td>
<td>3.0-3.6V</td>
</tr>
</tbody>
</table>

**AC CONDITIONS OF TEST**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise/Fall Time</td>
<td>5 ns</td>
</tr>
<tr>
<td>Output Load</td>
<td>CL = 30 pF</td>
</tr>
<tr>
<td></td>
<td>See Figures 15 and 16</td>
</tr>
</tbody>
</table>
# 4 Mbit Flash + 1 Mbit or 256 Kbit SRAM ComboMemory

**SST31LF041 / SST31LF041A / SST31LF043 / SST31LF043A**

Data Sheet

## TABLE 5: DC OPERATING CHARACTERISTICS (VDD = 3.0-3.6V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_DDD</td>
<td>Power Supply Current</td>
<td></td>
<td>Address input = VIL/VIH, at f=1/TC, Min, VDD=VDD Max, all DQs open</td>
</tr>
<tr>
<td></td>
<td>Read</td>
<td></td>
<td>OE#=VIL, WE#=VIH, BEF#=VIL, BES#=VIL</td>
</tr>
<tr>
<td></td>
<td>Flash</td>
<td>12 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SRAM</td>
<td>40 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Concurrent Operation</td>
<td>55 mA</td>
<td></td>
</tr>
<tr>
<td>I_SB</td>
<td>Standby VDD Current</td>
<td>30 µA</td>
<td>BEF#=VIL, BES#=VIL, VDD=VDD Max</td>
</tr>
<tr>
<td>I_L</td>
<td>Input Leakage Current</td>
<td>1 µA</td>
<td>V_IN=GND to VDD, VDD=VDD Max</td>
</tr>
<tr>
<td>I_O</td>
<td>Output Leakage Current</td>
<td>1 µA</td>
<td>V_OUT=GND to VDD, VDD=VDD Max</td>
</tr>
<tr>
<td>V_IL</td>
<td>Input Low Voltage</td>
<td>0.4 V</td>
<td>VDD = VDD Min</td>
</tr>
<tr>
<td>V_SH</td>
<td>Input High Voltage</td>
<td>0.7 VDD</td>
<td>VDD = VDD Max</td>
</tr>
<tr>
<td>V_HC</td>
<td>Input High Voltage (CMOS)</td>
<td>VDD-0.3</td>
<td>VDD = VDD Max</td>
</tr>
<tr>
<td>V_OL</td>
<td>Output Low Voltage</td>
<td>0.2 V</td>
<td>I_O = 100 µA, VDD = VDD Min</td>
</tr>
<tr>
<td>V_BO</td>
<td>Output High Voltage</td>
<td>VDD-0.2</td>
<td>I_O = -100 µA, VDD = VDD Min</td>
</tr>
<tr>
<td>V_H</td>
<td>Supervoltage for A9 pin</td>
<td>11.4</td>
<td>BEF#=OE#=VIL, WE#=VIH</td>
</tr>
<tr>
<td>I_H</td>
<td>Supervoltage Current for A9 pin</td>
<td>200 µA</td>
<td>BEF#=OE#=VIL, WE#=VIH, A9=V_H Max</td>
</tr>
</tbody>
</table>

1. Specification applies to commercial temperature devices only. This parameter may be higher for extended devices.

## TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>NPUR-READ</td>
<td>Power-up to Read Operation</td>
<td>100 µs</td>
<td>µs</td>
</tr>
<tr>
<td>NPUR-WRITE</td>
<td>Power-up to Write Operation</td>
<td>100 µs</td>
<td>µs</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

## TABLE 7: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Condition</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_I/O</td>
<td>I/O Pin Capacitance</td>
<td>V_I/O = 0V</td>
<td>12 pF</td>
</tr>
<tr>
<td>C_In</td>
<td>Input Capacitance</td>
<td>V_IN = 0V</td>
<td>6 pF</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

## TABLE 8: RELIABILITY CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum Specification</th>
<th>Units</th>
<th>Test Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>N_END</td>
<td>Endurance</td>
<td>10,000 Cycles</td>
<td></td>
<td>JEDEC Standard A117</td>
</tr>
<tr>
<td>T_DR</td>
<td>Data Retention</td>
<td>100 Years</td>
<td></td>
<td>JEDEC Standard A103</td>
</tr>
<tr>
<td>I_LTH</td>
<td>Latch Up</td>
<td>100 + I_DDD mA</td>
<td></td>
<td>JEDEC Standard 78</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
## AC CHARACTERISTICS

### TABLE 9: SRAM Memory Bank Cycle Timing Parameters (V<sub>DD</sub> = 3.0-3.6V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>SST31LF041/043-70</th>
<th>SST31LF041A/043A-300</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>TRCS</td>
<td>Read Cycle Time</td>
<td>70</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>TBES</td>
<td>Bank Enable Access Time</td>
<td>70</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>TAAS</td>
<td>Address Access Time</td>
<td>70</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>TOES&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Output Enable Access Time</td>
<td>35</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>TBLZS&lt;sup&gt;2&lt;/sup&gt;</td>
<td>BES# to Active Output</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TOLZS&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Output Enable to Active Output</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TBLHZS&lt;sup&gt;1&lt;/sup&gt;</td>
<td>BES# to High-Z Output</td>
<td>25</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>TOHZS&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Output Disable to High-Z Output</td>
<td>25</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>TOHS</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

1. No TOES value for SST31LF041A/043A
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

### TABLE 10: SRAM Memory Bank Write Cycle Timing Parameters (V<sub>DD</sub> = 3.0-3.6V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>SST31LF041/043-70</th>
<th>SST31LF041A/043A-300</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>TWCS</td>
<td>Write Cycle Time</td>
<td>70</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>TBEW</td>
<td>Bank Enable to End-of-Write</td>
<td>60</td>
<td>230</td>
<td></td>
</tr>
<tr>
<td>TAWS</td>
<td>Address Valid to End-of-Write</td>
<td>60</td>
<td>230</td>
<td></td>
</tr>
<tr>
<td>TASTS</td>
<td>Address Set-up Time</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TWPS</td>
<td>Write Pulse Width</td>
<td>60</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>TWR</td>
<td>Write Recovery Time</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TDS</td>
<td>Data Set-up Time</td>
<td>30</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>TDH</td>
<td>Data Hold from Write Time</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

### TABLE 11: Flash Read Cycle Timing Parameters (V<sub>DD</sub> = 3.0-3.6V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>SST31LF041/043-70</th>
<th>SST31LF041A/043A-300</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>TRC</td>
<td>Read Cycle Time</td>
<td>70</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>TBE</td>
<td>Bank Enable Access Time</td>
<td>70</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>TAA</td>
<td>Address Access Time</td>
<td>70</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>TOE</td>
<td>Output Enable Access Time</td>
<td>40</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>TBLZ&lt;sup&gt;1&lt;/sup&gt;</td>
<td>BEF# Low to Active Output</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TOLZ&lt;sup&gt;1&lt;/sup&gt;</td>
<td>OE# Low to Active Output</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TBLHZ&lt;sup&gt;1&lt;/sup&gt;</td>
<td>BEF# High to High-Z Output</td>
<td>15</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>TOHZ&lt;sup&gt;1&lt;/sup&gt;</td>
<td>OE# High to High-Z Output</td>
<td>15</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>TOH</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
**TABLE 12: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS (V\textsubscript{DD} = 3.0-3.6V)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>SST31LF041/043-70</th>
<th>SST31LF041A/043A-300</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>T\textsubscript{BP}</td>
<td>Byte-Program Time</td>
<td>20</td>
<td>20</td>
<td>µs</td>
</tr>
<tr>
<td>T\textsubscript{AS}</td>
<td>Address Setup Time</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{AH}</td>
<td>Address Hold Time</td>
<td>30</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{BS}</td>
<td>WE# and BEF# Setup Time</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{BH}</td>
<td>WE# and BEF# Hold Time</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{OES}</td>
<td>OE# High Setup Time</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{OEH}</td>
<td>OE# High Hold Time</td>
<td>10</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{BP}</td>
<td>BEF# Pulse Width</td>
<td>40</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{WP}</td>
<td>WE# Pulse Width</td>
<td>40</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{WPH}</td>
<td>WE# Pulse Width High</td>
<td>30</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{BPH}</td>
<td>BEF# Pulse Width High</td>
<td>30</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{DS}</td>
<td>Data Setup Time</td>
<td>40</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{DH}</td>
<td>Data Hold Time</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{IDA}</td>
<td>Software ID Access and Exit Time</td>
<td>150</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>T\textsubscript{SE}</td>
<td>Sector-Erase</td>
<td>25</td>
<td>25</td>
<td>ms</td>
</tr>
<tr>
<td>T\textsubscript{SBE}</td>
<td>Bank-Erase</td>
<td>100</td>
<td>100</td>
<td>ms</td>
</tr>
<tr>
<td>T\textsubscript{BS}</td>
<td>Bank Enable Setup Time for Concurrent Operation</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
</tbody>
</table>
FIGURE 3: SRAM READ CYCLE TIMING DIAGRAM

FIGURE 4: SRAM WRITE CYCLE TIMING DIAGRAM
4 Mbit Flash + 1 Mbit or 256 Kbit SRAM ComboMemory
SST31LF041 / SST31LF041A / SST31LF043 / SST31LF043A

Data Sheet

FIGURE 5: FLASH READ CYCLE TIMING DIAGRAM

Note 1. For SST31LF041A/043A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 6: FLASH WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

Note 1. For SST31LF041A/043A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.
FIGURE 7: BEF# CONTROLLED FLASH PROGRAM CYCLE TIMING DIAGRAM

Note 1. For SST31LF041A/043A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 8: FLASH DATA# POLLING TIMING DIAGRAM

Note 1. For SST31LF041A/043A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.
FIGURE 9: FLASH TOGGLE BIT TIMING DIAGRAM

Note 1. For SST31LF041A/043A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 10: WE# CONTROLLED FLASH SECTOR-ERASE TIMING DIAGRAM

Note: The device also supports BEF# controlled Sector-Erase operation. The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 12)

SAX = Sector Address

Note 1. For SST31LF041A/043A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.
FIGURE 11: WE# CONTROLLED FLASH BANK-ERASE TIMING DIAGRAM

FIGURE 12: FLASH SOFTWARE ID ENTRY AND READ

Note 1. For SST31LF041A/043A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

Note: Device ID = 16H for SST31LF041A, 17H for SST31LF041, 65H for SST31LF043 and 66H for SST31LF043A.
THREE-BYTE SEQUENCE FOR SOFTWARE ID EXIT AND RESET

ADDRESS A_{14-0}  
5555 2AAA 5555

BES#

DQ_{7-0}  
AA 55 F0

BEF#

OE#^1

WE#

SW0 SW1 SW2  
5555 2AAA 5555

T_{IDA}

T_{WP}

T_{WHP}

Note 1. For SST31LF041A/043A, BES# and OE# share pin 32. During Flash operation, pin 32 functions as OE#.

FIGURE 13: FLASH SOFTWARE ID EXIT AND RESET

ADDRESS A_{18-0}  
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

BEj#

BEj1#

WE#

OE#

DQ_{7-0}  
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

Note:  
j = F or S  
j1 = S or F

FIGURE 14: TIMING DIAGRAM FOR ALTERNATING BETWEEN FLASH/SRAM AND SRAM/FLASH
AC test inputs are driven at \( V_{\text{IHT}} \) (0.9 \( V_{\text{DD}} \)) for a logic “1” and \( V_{\text{ILT}} \) (0.1 \( V_{\text{DD}} \)) for a logic “0”. Measurement reference points for inputs and outputs are \( V_{\text{IT}} \) (0.5 \( V_{\text{DD}} \)) and \( V_{\text{OT}} \) (0.5 \( V_{\text{DD}} \)). Input rise and fall times (10% ↔ 90%) are <5 ns.

**Note:**

- \( V_{\text{IT}} \) - \( V_{\text{INPUT Test}} \)
- \( V_{\text{OT}} \) - \( V_{\text{OUTPUT Test}} \)
- \( V_{\text{IHT}} \) - \( V_{\text{INPUT HIGH Test}} \)
- \( V_{\text{ILT}} \) - \( V_{\text{INPUT LOW Test}} \)

**FIGURE 15: AC INPUT/OUTPUT REFERENCE WAVEFORMS**

**FIGURE 16: A TEST LOAD EXAMPLE**
FIGURE 17: BYTE-PROGRAM ALGORITHM

Start

Load data: AAH
Address: 5555H

Load data: 55H
Address: 2AAAH

Load data: A0H
Address: 5555H

Load Byte
Address/Byte
Data

Wait for end of
Program (TBP,
Data# Polling
bit, or Toggle bit
operation)

Program Completed
FIGURE 18: WAIT OPTIONS

**Internal Timer**
- Byte Program/Erase Initiated
  - Wait \( T_{BP} \), \( T_{SBE} \), or \( T_{SE} \)
  - Program/Erase Completed

**Toggle Bit**
- Byte Program/Erase Initiated
  - Read byte
  - Read same byte
  - Does DQ6 match?
    - No
      - Program/Erase Completed
    - Yes
      - Program/Erase Completed

**Data# Polling**
- Byte Program/Erase Initiated
  - Read DQ7
  - Is DQ7 = true data?
    - No
      - Program/Erase Completed
    - Yes
      - Program/Erase Completed
FIGURE 19: SOFTWARE PRODUCT COMMAND FLOWCHARTS
FIGURE 20: ERASE COMMAND SEQUENCE

**Chip-Erase Command Sequence**

1. Load data: AAH
   Address: 5555H

2. Load data: 55H
   Address: 2AAA AH

3. Load data: 80H
   Address: 5555H

4. Load data: AAH
   Address: 5555H

5. Load data: 55H
   Address: 2AAA AH

6. Load data: 10H
   Address: 5555H

7. Load data: AAH
   Address: 5555H

8. Wait TSBE

9. Chip erased to FFH

**Sector-Erase Command Sequence**

1. Load data: AAH
   Address: 5555H

2. Load data: 55H
   Address: 2AAA AH

3. Load data: 80H
   Address: 5555H

4. Load data: 55H
   Address: 2AAA AH

5. Load data: 30H
   Address: SAx

6. Load data: AAH
   Address: 5555H

7. Wait TSE

8. Sector erased to FFH
### 4 Mbit Flash + 1 Mbit or 256 Kbit SRAM ComboMemory

**SST31LF041 / SST31LF041A / SST31LF043 / SST31LF043A**

#### Device Speed Suffix1 Suffix2

<table>
<thead>
<tr>
<th>Device</th>
<th>Speed</th>
<th>Suffix1</th>
<th>Suffix2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SST31LF04xx</td>
<td>XXX</td>
<td>XX</td>
<td>XX</td>
</tr>
</tbody>
</table>

**Package Modifier**

- **H** = 32 leads
- **I** = 40 leads
- **Numeric** = Die modifier

**Package Type**

- **W** = TSOP (8mm x 14mm - 32-lead package)
- **(10mm x 14mm - 40-lead package)**

**Temperature Range**

- **C** = Commercial = 0°C to +70°C
- **E** = Extended = -20°C to +85°C

**Minimum Endurance**

- 4 = 10,000 cycles

**Read Access Speed**

- 70 = 70 ns
- 300 = 300 ns

**Version**

- **A** = 32-lead TSOP Package

**Density**

- 041/041A = 4 Mbit Flash + 1 Mbit SRAM
- 043/043A = 4 Mbit Flash + 256 Kbit SRAM

**Voltage**

- **L** = 3.0-3.6V

**Device Family**

- 31 = Monolithic ComboMemory

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**SST31LF041 Valid combinations**

- SST31LF041-70-4C-WI
- SST31LF041-70-4E-WI

**SST31LF041A Valid combinations**

- SST31LF041A-300-4C-WH
- SST31LF041A-300-4E-WH

**SST31LF043 Valid combinations**

- SST31LF043-70-4C-WI
- SST31LF043-70-4E-WI

**SST31LF043A Valid combinations**

- SST31LF043A-300-4C-WH
- SST31LF043A-300-4E-WH

**Example:**

Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.
PACKAGING DIAGRAMS

Note:
1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±.05) mm.
4. Maximum allowable mold flash is 0.15mm at the package ends, and 0.25mm between leads.

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH
4 Mbit Flash + 1 Mbit or 256 Kbit SRAM ComboMemory
SST31LF041 / SST31LF041A / SST31LF043 / SST31LF043A

Note: 1. Complies with JEDEC publication 95 MO-142 CA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±.05) mm.
4. Maximum allowable mold flash is 0.15mm at the package ends, and 0.25mm between leads.

40-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 10MM X 14MM
SST PACKAGE CODE: WI